Claims

[c1] What is claimed is:

1. A timer lockout circuit comprising:

a delay circuit for receiving and delaying a first timing signal;

a first circuit for receiving said first timing signal from said first delay circuit and for latching said first timing signal;

a programmable timing circuit for receiving said first timing signal from said first circuit and for delaying said first timing signal by a programmable time interval;

a one-shot generator for receiving said first timing signal from said programmable timing circuit and for generating a set signal;

a second circuit for receiving said set signal from said one-shot generator and for latching said set signal;

a third circuit for receiving a second timing signal and for latching said second timing signal;

a combinational logic circuit for receiving said set signal from said second circuit and for receiving said second timing signal from said third circuit and for generating a third timing signal; and

a second delay circuit for receiving and delaying said third timing signal and for simultaneously resetting said first circuit, said second circuit and said third circuit after delaying said third timing signal.

[c2] 2. The circuit of claim 1, wherein said programmable timing circuit resets to zero elapsed time upon de-assertion of said first timing signal if said programmable interval has not been reached prior to said de-assertion of said first timing signal.

[c3] 3. The circuit of claim 1, wherein said programmable time interval is determined by a digital signal changing the state of fuses or antifuses.

[c4] 4. The circuit of claim 1, further including an inverter for receiving said first timing signal, inverting said first timing signal and for applying said inverted timing signal to a reset input of said first circuit.

[c5] 5. The circuit of claim 1, wherein said second delay circuit applies said third timing signal to said reset inputs of said first circuit, said second circuit and said third circuit.

[c6] 6. The circuit of claim 1, wherein said combinational logic circuit is an AND gate.

[c7] 7. A timer lockout circuit comprising:

first means for receiving a first timing signal from a first delay circuit and for latching said first timing signal;

second means for receiving said first timing signal from said first means and for delaying said first timing signal by a programmable time interval;

third means for receiving said first timing signal from said second means and for generating a set signal;

fourth means for receiving said set signal from said third means and for latching said set signal;

fifth means for receiving a second timing signal and for latching said second timing signal;

sixth means for receiving said set signal from said fourth means and for receiving said second timing signal from said fifth means and for

ting a third timing signal; and

seventh means for simultaneously resetting said first means, said fourth means and said fifth means.

[c8] 8. The circuit of claim 7, further including an eighth means for receiving said first timing signal, inverting said first timing signal and for applying said inverted timing signal to a reset input of said first circuit.

[c9] 9. The circuit of claim 7, further including a ninth means for delaying said third timing signal prior to applying said third timing signal to reset inputs of said first means, fourth means and fifth means.

[c10] 10. The circuit of claim 7, further including a fuse or antifuse circuit for generating a digital signal to set said programmable time interval.

[c11] 11. A SDRAM comprising:

at least one bank of DRAM cells;

said SDRAM operable to a first specification defined by a first clock frequency, a first write recovery time and a first time interval for precharge to row address strobe; and

means for programming said SDRAM operable to a second specification defined by a second clock frequency, a second write recovery time and a second time interval for precharge to row address strobe.

[c12] 12. The SDRAM of claim 11, wherein precharging of bitlines in said at least one bank of DRAM cells is delayed by a time interval substantially equal to the difference between said first write recovery time and said second write recovery time.

[c13] 13. The SDRAM of claim 12, wherein said second write recovery time is less than said first write recovery time.

[c14] 14. The SDRAM of claim 12, wherein the sum of a minimum internal time to write a DRAM cell of said at least one bank of DRAM cells and a minimum internal time to precharge a bitline connected to said DRAM cell is the same when said SDRAM is operable to said first specification or to said second specification.

[c15] 15. The SDRAM of claim 12, wherein the sum of said first write recovery time and said first time interval for precharge to row address strobe is equal to the sum of said second write recovery time and said second time interval for precharge to row address strobe.

[c16] 16.The SDRAM of claim 12, wherein:
said first clock frequency is 1/7.5 nanoseconds, said first write recovery time is 15 nanoseconds and said first time interval for precharge to row address strobe is 15 nanoseconds; and
said second clock frequency is 1/6 nanoseconds, said first write recovery time is 15 nanoseconds and said first time interval for precharge to row address strobe is 18 nanoseconds.

[c17] 17. A SDRAM comprising:
at least one bank of DRAM cells;
said SDRAM operable to a first write recovery time;
a first circuit for programming said SDRAM operable to a second write recovery time; and

a second circuit for delaying the start of a precharge command for a time interval equal to said first write recovery time when said SDRAM is operable to said second write recovery time.

[c18] 18.The SDRAM of claim 17, wherein said SDRAM is operable to a first specification defined by a first clock frequency, said first write recovery time and a first time interval for precharge to row address strobe and said SDRAM is operable to a second specification defined by a second clock frequency, said second write recovery time and a second time interval for precharge to row address strobe.

[c19] 19. The SDRAM of claim 18, wherein said first circuit for programming said SDRAM delays precharging of bitlines in said at least one bank of DRAM cells by a time interval substantially equal to the difference between said first write recovery time and said second write recovery time.

[c20] 20. The SDRAM of claim 17, wherein said second write recovery time is less than said first write recovery time.

[c21] 21. The SDRAM of claim 17, wherein said first circuit for programming said SDRAM operable to a second write recovery time comprises:
a first delay circuit for receiving and delaying a first timing signal;
a first latch for receiving a first timing signal from said first delay circuit and for latching said first timing signal, said first timing signal indicating a fixed number of data bits have been written to said at least one bank of DRAM cells;
a programmable timer for receiving said first timing signal from said first

latch and for delaying said first timing signal by a programmable time interval;

a one shot pulse generator for receiving said first timing signal from said programmable timer and for generating a set signal;

a second latch for receiving said set signal from said one shot pulse generator and for latching said set signal;

a third latch for receiving a second timing signal and for latching said second timing signal, said second timing signal being a signal to turn off wordlines in said at least one bank of DRAM cells;

a logic gate for receiving said set signal from said second latch, for receiving said second timing signal from said third latch and for generating a third timing signal, said third timing signal being a delayed signal to turn off wordlines in said at least one bank of DRAM cells; and

a second delay circuit for receiving and delaying said third timing signal and for simultaneously resetting said first latch, said second latch and said third latch after delaying said third timing signal.

[c22] 22. The SDRAM of claim 21, wherein said programmable timer resets to zero elapsed time upon de-assertion of said first timing signal if said programmable interval has not been reached prior to said de-assertion of said first timing signal

[c23] 23. The SDRAM of claim 21, wherein said programmable time interval is determined by a digital signal changing the state of fuses or antifuses.

[c24] 24. The SDRAM of claim 21, further including an inverter for receiving said first timing signal, inverting said first timing signal and for applying

said inverted timing signal to a reset input of said first latch.

[c25] 25. The SDRAM of claim 21, wherein said second delay circuit applies said third timing signal to reset inputs of said first, second and third latches.

[c26] 26. The SDRAM of claim 21, wherein said logic gate is an AND gate.